X20DC1176

1 General information

The module is equipped with 1 input for an ABR incremental encoder with RS422-based output signals and 5 V encoder supply. The encoder inputs are monitored (A, B, R, A\, B\, R\).

- 1 ABR incremental encoder 5 V
- Encoder input monitoring
- 2 additional inputs, e.g. for latch input
- 5 VDC, 24 VDC and GND for encoder supply
- NetTime timestamp: Counter change
- Can be used with a SafeLOGIC controller

NetTime timestamp of the counter

For many applications, not only the counter value is important, but also the exact time of the counter change. For this purpose, the module has a NetTime function that provides the recorded counter value with a timestamp accurate to microseconds.

The module provides the PLC with the counter value and timestamp as an absolute time value. The NetTime mechanisms ensure that the PLC NetTime clock and the local NetTime clock on the module have the same absolute time at all times.

2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC1176	X20 digital counter module, 1 ABR incremental encoder, 5 V, 600 kHz input frequency, 4x evaluation, encoder monitoring, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20DC1176 - Order data

3 Technical data

Model number	X20DC1176
Short description	
I/O module	1 ABR incremental encoder 5 V
General information	
B&R ID code	0xA706
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Power consumption	
Bus	0.01 W
Internal I/O	1 W
Additional power dissipation caused by actuators (resistive) [W]	-
Type of signal lines	Shielded cables must be used for all signal lines.
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input characteristics per EN 61131-2	Type 1
Input voltage	24 VDC -15% / +20%
Input current at 24 VDC	Approx. 3.3 mA
Input circuit	Sink
Input filter	
Hardware	≤2 µs
Software	-
Connection type	3-wire connections
Input resistance	7.03 kΩ
Additional functions	Latch input
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
ABR incremental encoder	
Encoder inputs	5 V, symmetrical
Counter size	16/32-bit
Input frequency	Max. 600 kHz
Evaluation	4x
Minimum diff. slew rate	1 V/µs
Encoder power supply	
5 VDC	±5%, module-internal, max. 300 mA
24 VDC	Module-internal, max. 300 mA
Input filter	
Hardware	≤400 ns
Software	-
Switching threshold	
Low	>1 V
Common-mode range	$-10\ V \le V_{CM} \le +13.2\ V$
Overload characteristics of encoder power supply	Short-circuit proof, overload-proof
Isolation voltage between encoder and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel

Table 2: X20DC1176 - Technical data

Model number	X20DC1176
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Spacing	$12.5^{+0.2}$ mm

Table 2: X20DC1176 - Technical data

4 LED status indicators

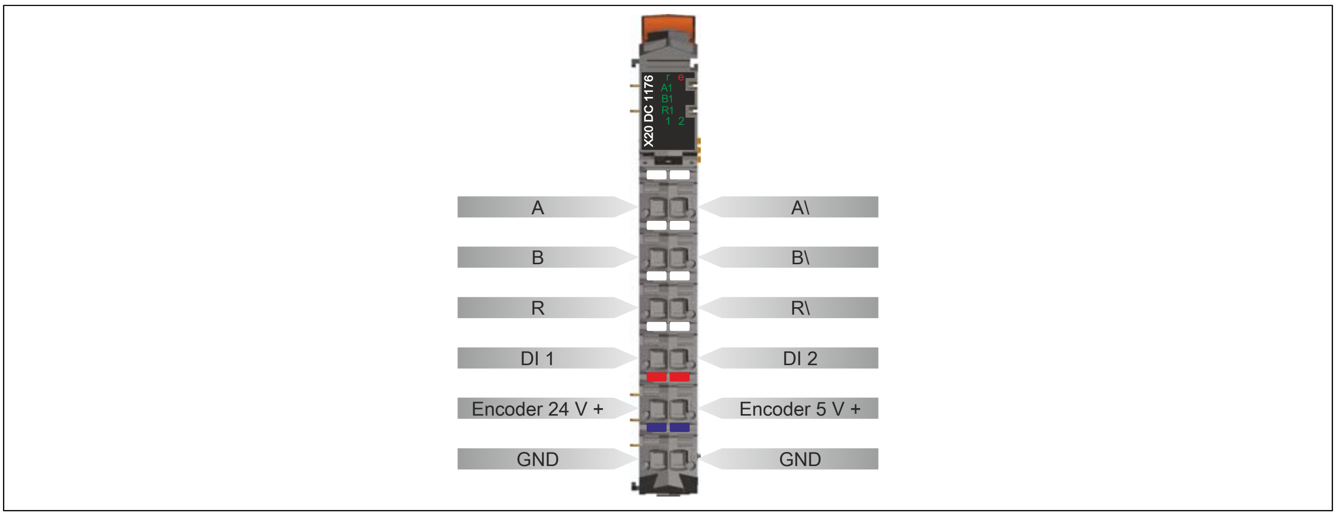
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" of the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	The encoder monitor has detected a line fault on the encoder inputs. The status bits must be evaluated in order to provide a more detailed definition of this error. The following error states are detected: • Open line • Short-circuit or voltage level too low
			On	Error or reset status
	A1	Green		Input state of counter input A
	B1	Green		Input state of counter input B
	R1	Green		Input state of reference pulse R
	1 - 2	Green		Input state of the corresponding digital input

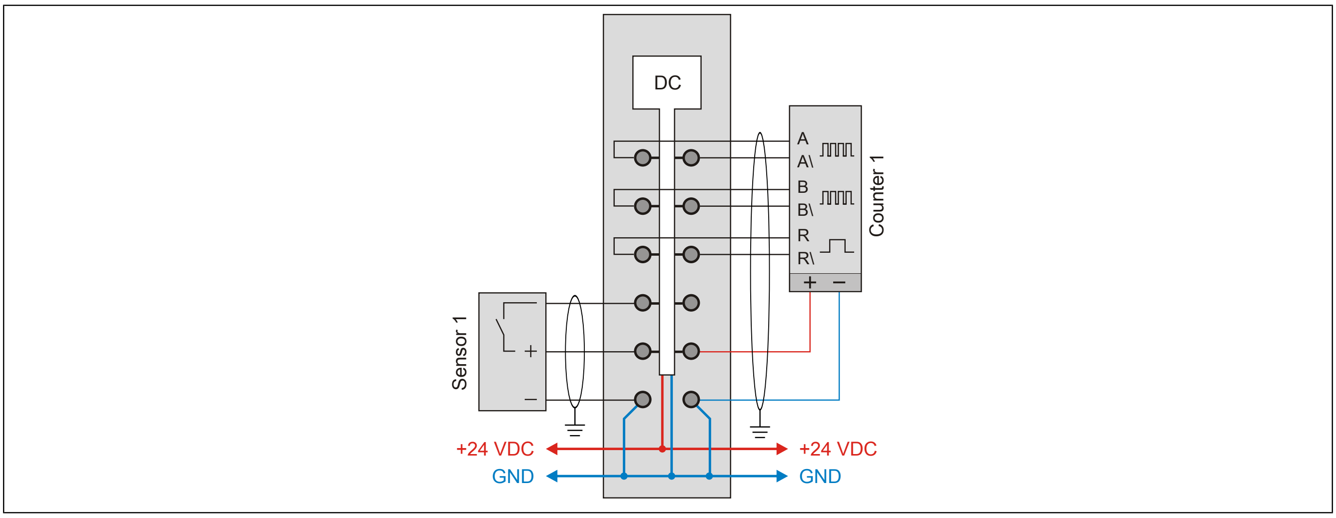
1) Depending on the configuration, a firmware update can take up to several minutes.

5 Pinout

Shielded cables must be used for all signal lines.

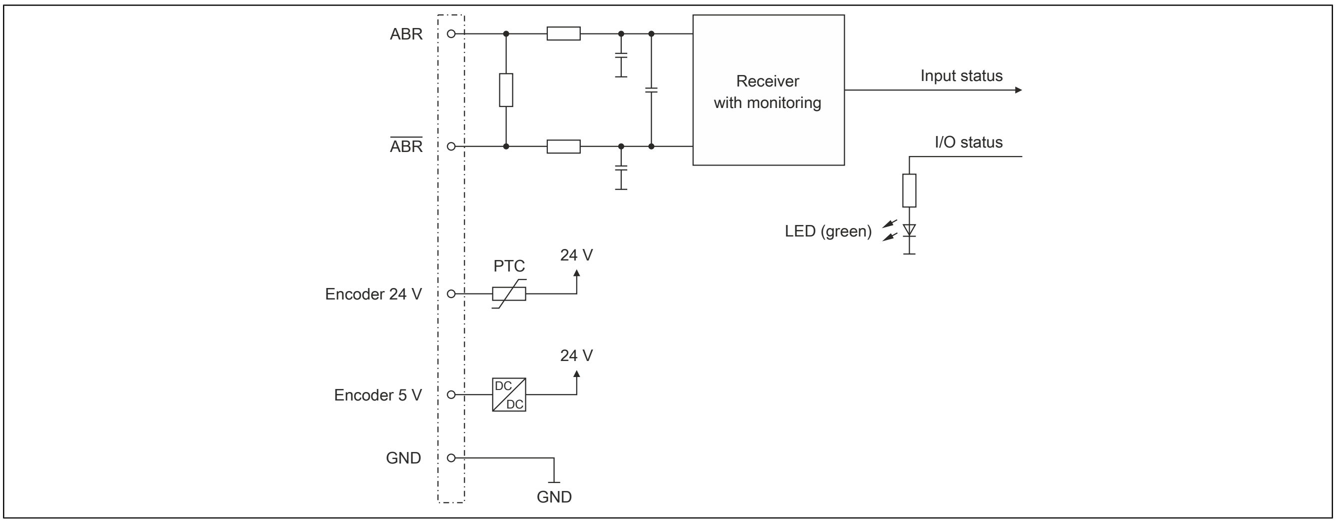


6 Connection example

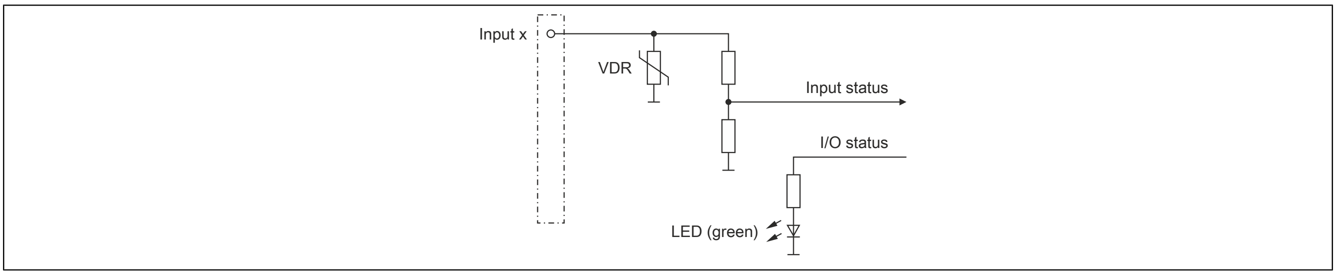


7 Input circuit diagram

Counter inputs



Standard inputs



8 Register description

8.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" of the X20 system user's manual.

8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
513	CfO_SIframeGenID	USINT				•
642	CfO_SystemCycleTime	UINT				•
769	CfO_PhyIOConfigCh01	USINT				•
771	CfO_PhyIOConfigCh02	USINT				•
773	CfO_PhyIOConfigCh03	USINT				•
777	CfO_PhyIOConfigCh04	USINT				•
779	CfO_PhyIOConfigCh05	USINT				•
815	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	CfO_BWQuitTime_0	UDINT				•
6145	CfO_CounterCycleSelect	USINT				•
6147	CfO_CounterMode	USINT				•
6149	CfO_LatchMode	USINT				•
6151	CfO_LatchComparator	USINT				•
6159	CfO_BWCNTEnableMaskChannel7_0	USINT				•
Communication						
683	SDCLifeCount	SINT	•			
6342	Encoder01	INT	•			
6340		DINT				
6310	Encoder01TimeValid	INT	•			
6308		DINT				
6358	Encoder01Latch	INT	•			
6356		DINT				
6153	Encoder commands	USINT			•	
	Encoder01Reset	Bit 0				
	Encoder01LatchEnable	Bit 1				
927	Input status of signal lines	USINT	•			
	Encoder01_A	Bit 0				
	Encoder01_B	Bit 1				
	Encoder01_R	Bit 2				
	DigitalInput01	Bit 4				
	DigitalInput02	Bit 5				
847	Status of signal lines	USINT	•			
	BW_Channel_A	Bit 0				
	BW_Channel_B	Bit 1				
	BW_Channel_R	Bit 2				
811	Acknowledging error status of signal lines	USINT			•	
	BW_QuitChannel_A	Bit 0				
	BW_QuitChannel_B	Bit 1				
	BW_QuitChannel_R	Bit 2				
6326	Encoder01TimeChanged	INT	•			
6324		DINT				
6303	Encoder01LatchCount	SINT	•			
843	Status of encoder supplies	USINT	•			
	PowerSupply01	Bit 0				
	PowerSupply02	Bit 1				

SafeLOGIC registers

This module contains additional registers that allow the module to be used with a SafeLOGIC controller.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
7170	CfO_DTS_SourceRef	INT				•
7173	CfO_DTS_CycleSelect	USINT				•
Communication						
7188	Encoder01	DINT	•			
7196	Encoder01TimeValid	DINT	•			
7202	DTS_SourceRef	INT	•			
7206	DTS_CheckSum	INT	•			

8.3 Function model 254 - Bus controller

Register	Offset[1]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
513	-	CfO_SIframeGenID	USINT				•
642	-	CfO_SystemCycleTime	UINT				•
769	-	CfO_PhyIOConfigCh01	USINT				•
771	-	CfO_PhyIOConfigCh02	USINT				•
773	-	CfO_PhyIOConfigCh03	USINT				•
777	-	CfO_PhyIOConfigCh04	USINT				•
779	-	CfO_PhyIOConfigCh05	USINT				•
815	-	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	-	CfO_BWQuitTime_0	UDINT				•
6145	-	CfO_CounterCycleSelect	USINT				•
6147	-	CfO_CounterMode	USINT				•
6149	-	CfO_LatchMode	USINT				•
6151	-	CfO_LatchComparator	USINT				•
6159	-	CfO_BWCNTEnableMaskChannel7_0	USINT				•
Communication							
6342	0	Encoder01	INT	•			
6310	2	Encoder01TimeValid	INT	•			
6358	4	Encoder01Latch	INT	•			
6153	1	Encoder commands	USINT			•	
		Encoder01Reset	Bit 0				
		Encoder01LatchEnable	Bit 1				
927	7	Input status of signal lines	USINT	•			
		Encoder01_A	Bit 0				
		Encoder01_B	Bit 1				
		Encoder01_R	Bit 2				
		DigitalInput01	Bit 4				
		DigitalInput02	Bit 5				
847	6	Status of signal lines	USINT	•			
		BW_Channel_A	Bit 0				
		BW_Channel_B	Bit 1				
		BW_Channel_R	Bit 2				
811	0	Acknowledging error status of signal lines	USINT			•	
		BW_QuitChannel_A	Bit 0				
		BW_QuitChannel_B	Bit 1				
		BW_QuitChannel_R	Bit 2				
6326	-	Encoder01TimeChanged	INT		•		
6303	-	Encoder01LatchCount	SINT		•		
843	-	Status of encoder supplies	USINT		•		
		PowerSupply01	Bit 0				
		PowerSupply02	Bit 1				

1) The offset specifies the position of the register within the CAN object.

8.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use additional registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" of the X20 user's manual (version 3.50 or later).

8.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

8.4 Encoder - Configuration

The following registers are used for setting functions and configuring the module.

8.4.1 Enabling error monitoring for the signal lines

Name:
CfO_BWCNTEnableMaskChannel7_0

This register requires individually enabling error monitoring for each of the signal channels. "Open line", "short circuit" and "voltage level too low" are reported as error states. Any errors that occur are reported in the error status registers "BW_Channel_x" on page 13.

Data type	Value	Bus controller default setting
USINT	See bit structure.	7

Bit structure:

Bit	Name	Value	Information
0	Enable error monitoring for signal A lines	0	Error monitoring - Encoder Signal A disabled
		1	Error monitoring - Encoder signal A enabled (bus controller default setting)
1	Enable error monitoring for signal B lines	0	Error monitoring - Encoder Signal B disabled
		1	Error monitoring - Encoder signal B enabled (bus controller default setting)
2	Enable error monitoring for signal R lines	0	Error monitoring - Encoder Signal R disabled
		1	Error monitoring - Encoder signal R enabled (bus controller default setting)
3 - 7	Reserved	0	

8.4.2 Timing for automatic error acknowledgment

Name:
CfO_BWQuitTime_0

This register can be used to enable an additional automatic acknowledgment of the error status through timing. If a valid time is set, then the acknowledgment can still be made manually, the only difference is that automatic acknowledgment will take place on the module after the defined amount of time has passed. If the error state has not yet been corrected, then the error status remains and the time is reset. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages.
If the timing = 0, then acknowledgment is only possible using the cyclic acknowledgment registers.

Data type	Value	Information
UDINT	0	No automatic acknowledgment. Bus controller default setting
	1 to 2.147.483.647	Time for automatic acknowledgment [μs]

8.4.3 Setting the latch mode

Name:
CfO_LatchMode

This register is used to set the latch mode:

- Single shot latch mode:
  The latch function must be enabled/set. After a successful latch procedure, the activation must be reset in order for a new latch procedure to be activated.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired.

A changed counter state on "Encoder01LatchCount" on page 11 indicates that the latch procedure has been performed. The counter value is stored in the latch register "Encoder01Latch" on page 11.

Data type	Value	Information
USINT	0	Single-shot latch procedure (bus controller default setting)
	1	Continuous latch procedure

8.4.4 Signal channels for triggering latch procedure

Name:
CfO_LatchComparator

This register defines the signal channels and their level for triggering the latch procedure.

- This mainly configures which channels are linked to generate the latch event. All three signals from the encoder and digital input 1 can be used for the "AND" operation.
- The "active voltage level" needed for the latch procedure can now be used according to the physical signals.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Name	Value	Information
0	Defines signal level for encoder signal A	0	Low (bus controller default setting)
		1	High
1	Defines signal level for encoder signal B	0	Low (bus controller default setting)
		1	High
2	Defines signal level for encoder signal R	0	Low (bus controller default setting)
		1	High
3	Defines signal level for digital input 1	0	Low (bus controller default setting)
		1	High
4	Use encoder signal A to trigger latch procedure	0	Disabled (bus controller default setting)
		1	Latch function linked to encoder signal A
5	Use encoder signal B to trigger latch procedure	0	Disabled (bus controller default setting)
		1	Latch function linked to encoder signal B
6	Use encoder signal R to trigger latch procedure	0	Disabled (bus controller default setting)
		1	Latch function linked to encoder signal R
7	Use digital input 1 to trigger latch procedure	0	Disabled (bus controller default setting)
		1	Latch function linked to digital input 1

8.4.5 Physical configuration

The following registers must be set to the specified constant value for correct physical configuration:

8.4.5.1 Constant register "CfO_SIframeGenID"

Name:
CfO_SIframeGenID

Data type	Value	Information
USINT	9	Bus controller default setting

8.4.5.2 Constant register "CfO_SystemCycleTime"

Name:
CfO_SystemCycleTime

Cycle time of encoder acquisition in 1/8 µs steps. 1 encoder value is acquired as the counter value per cycle.

Data type	Value	Information
UINT	800	800 = 100 µs. Bus controller default setting

8.4.5.3 Constant register "CfO_PhyIOConfigCh0x"

Name:
CfO_PhyIOConfigCh01 to CfO_PhyIOConfigCh05

Data type	Value	Information
USINT	0	Bus controller default setting

8.4.5.4 Constant register "CfO_BWQuitTimeSelChannel7_0"

Name:
CfO_BWQuitTimeSelChannel7_0

Data type	Value	Information
USINT	0	Bus controller default setting

8.4.5.5 Constant register "CfO_CounterCycleSelect"

Name:
CfO_CounterCycleSelect

Data type	Value	Information
USINT	2	Bus controller default setting

8.4.5.6 Constant register "CfO_CounterMode"

Name:
CfO_CounterMode

Data type	Value	Information
USINT	3	Bus controller default setting

8.5 Encoder - Communication

8.5.1 Counter for verifying the data frame

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

8.5.2 Display of the counter state

Name:
Encoder01

The counter state of the incremental encoder is displayed as a 16 or 32-bit counter value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

8.5.3 NetTime of the last valid counter value

Name:
Encoder01TimeValid

The NetTime of the last valid counter value is the time of the last valid counter value recorded on the module (see register "Cfo_SystemCycleTime" on page 9). The user is able to determine the validity of the counter value by evaluating its age in the program. This means that the module and error status bits do not have to be checked additionally to determine the validity of the value.

The NetTime of the last valid counter value that was read is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

For more information about NetTime and timestamps, see "NetTime technology" on page 18.

Data type	Value	Information
INT	-32768 to 32767	NetTime in µs
DINT[1]	-2.147.483.648 to 2.147.483.647	

1) Can only be configured in the standard function model

8.5.4 NetTime of the last counter value change

Name:
Encoder01TimeChanged

For slow X2X Link cycles, the NetTime of the last counter value change can be used to determine the speed more accurately.

The NetTime of the last counter value change is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

For more information about NetTime and timestamps, see "NetTime technology" on page 18.

Data type	Value	Information
INT	-32768 to 32767	NetTime in µs
DINT[1]	-2.147.483.648 to 2.147.483.647	

1) Can only be configured in the standard function model

8.5.5 Counter value at the time of the last latch

Name:
Encoder01Latch

The counter value at the time of the last latch is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

8.5.6 Counter value of latch event

Name:
Encoder01LatchCount

The latch events are counted and stored in a cyclic 8-bit counter. This counter is incremented with each latch event, thereby indicating a new occurrence. The new latched counter value is stored in the respective latch register.

Data type	Value
SINT	-128 to 127

8.5.7 Encoder commands

Name:
Encoder01Command

This register can be used to

1) reset the counter value. The counter is kept at zero until this command is reset.
2) enable the latch procedure. If the latch configuration is valid and matches the hardware signals, then this activation causes the counter value to be saved in the latch register.

The two different latch configurations that are possible (see "Setting the latch mode" on page 8) must be handled as follows:

- Single shot latch mode:
  After successful latching, indicated by the latch event counter, activation must be reset before any more latching is possible. The activation must be set again if additional latching is needed.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired. The latch event counter is incremented with each event.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01Reset	0	Do not reset
		1	Set encoder value to 0
1	Encoder01LatchEnable	0	Do not activate latch
		1	Latching
2 - 7	Reserved	0	

8.5.8 Input status of signal lines

Name:
Encoder01_A
Encoder01_B
Encoder01_R
DigitalInput01 to DigitalInput02

This register displays the input status of the signal lines from the encoder and the digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01_A	0/1	Input state of encoder signal A
1	Encoder01_B	0/1	Input state of encoder signal B
2	Encoder01_R	0/1	Input state of encoder signal R
3	Reserved	0	
4	DigitalInput01	0/1	Input state - Digital input 1
5	DigitalInput02	0/1	Input state - Digital input 2
6 - 7	Reserved	0	

8.5.9 Error status of signal lines

The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

8.5.9.1 Status of signal lines

Name:
BW_Channel_A
BW_Channel_B
BW_Channel_R

This register displays the error states of the signal lines from the encoder. The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_Channel_A	0	No error in encoder signal A
		1	Open line, short circuit or voltage level too low
1	BW_Channel_B	0	No error in encoder signal B
		1	Open line, short circuit or voltage level too low
2	BW_Channel_R	0	No error in encoder signal R
		1	Open line, short circuit or voltage level too low
3 - 7	Reserved	0	

8.5.9.2 Acknowledging error status of signal lines

Name:
BW_QuitChannel_A
BW_QuitChannel_B
BW_QuitChannel_R

This register can be used to acknowledge the latched error states of the signal lines from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bits must also be reset or else any repetition of the error would be undetected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_QuitChannel_A	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal A
1	BW_QuitChannel_B	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal B
2	BW_QuitChannel_R	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal R
3 - 7	Reserved	0	

8.5.9.3 Manual acknowledgment of latched error states

The latched error states of the signal lines from the encoder can be acknowledged manually. However, if there are still pending errors remaining, then the error status remains active. After successfully acknowledging the errors (latched error status = 0), the acknowledge bits must still be reset by the user or else a re-occurrence of an error could be overlooked by the user.

Example 1: **Cause of error corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user after the cause of error has been corrected. The latched error status changes to zero.

The manual acknowledge must now be reset so that any new errors will be recognized by the user.

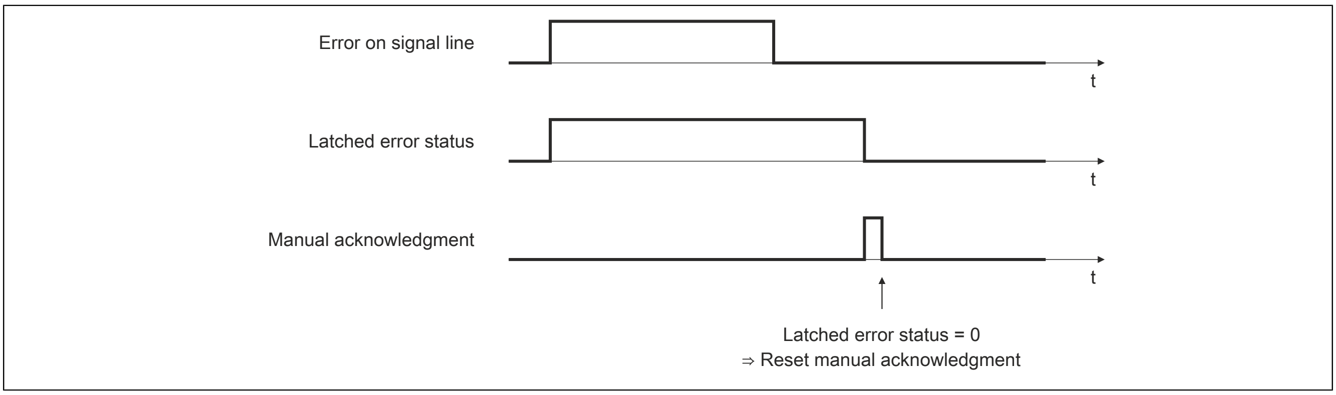


Figure 1: Cause of error corrected before being acknowledged

Example 2: **Cause of error not yet corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user before the cause of error has been corrected. The latched error status remains set because the error is still remaining.

Acknowledgment is only successful after the cause of error has been corrected. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

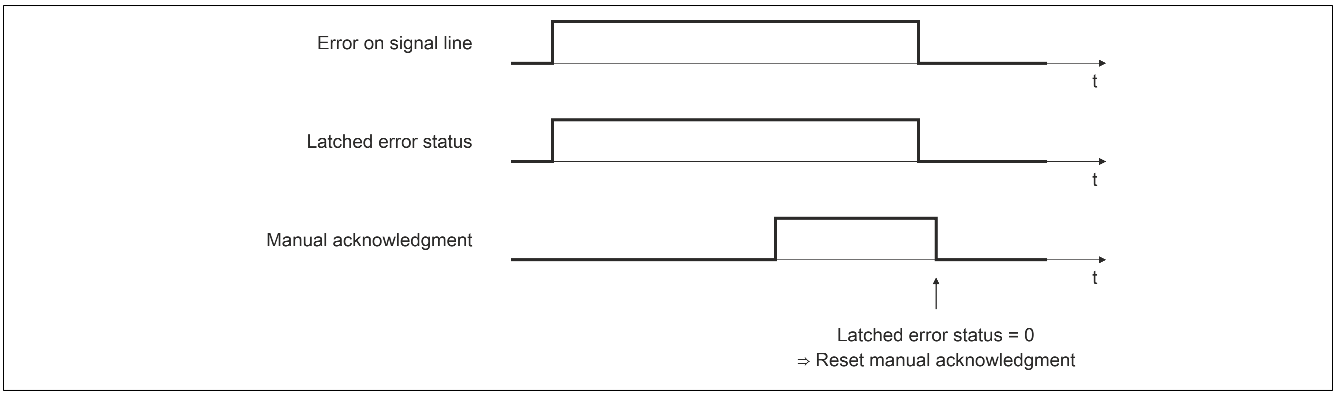


Figure 2: Cause of error not yet corrected before being acknowledged

8.5.9.4 Automatic acknowledgment of latched error states

In addition to manual acknowledgment, automatic acknowledgment of the latched error states after a specified amount of time can also be enabled. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages and for the validity of the counter value to be determined using its age.

If the time specification = 0, then only manual acknowledgment is possible.

Example 1: An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged as soon as the time expires. The latched error status changes to zero.

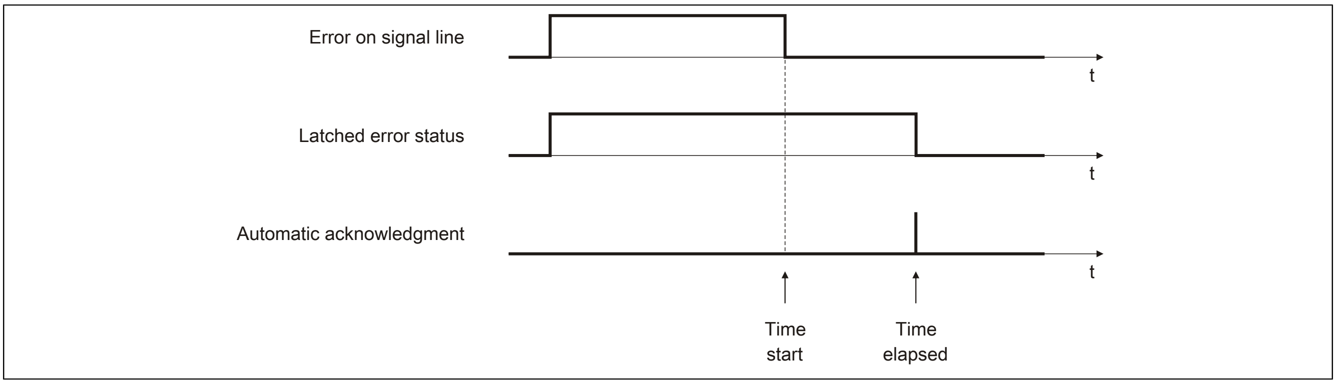


Figure 3: Latched error state acknowledged automatically

Example 2: Automatic and manual acknowledge used

An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged manually by the user before the time expires. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

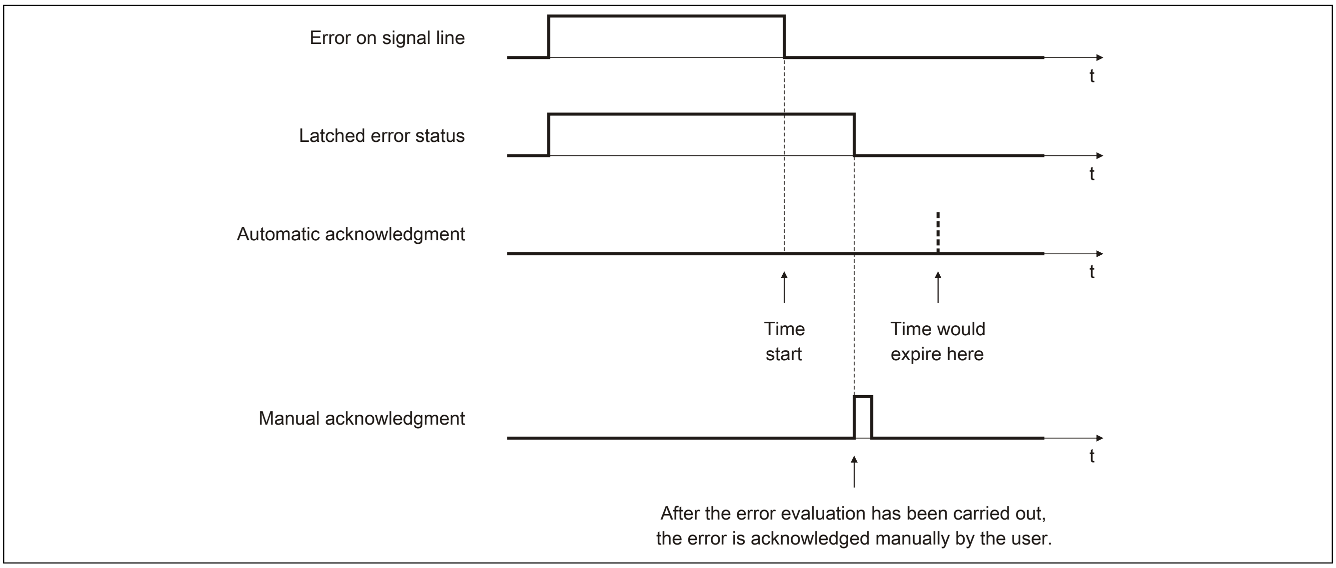


Figure 4: Automatic and manual acknowledge used

8.5.10 Status of encoder supplies

Name:
PowerSupply01 to PowerSupply02

This register shows the status of the integrated encoder supplies. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1	PowerSupply02	0	5 VDC encoder power supply OK
		1	5 VDC encoder power supply faulty
2 - 7	Reserved	-	

8.6 DATA_to_SafeDATA

Function DATA_to_SafeDATA determines a safe signal from 2 independent standard signals. For this purpose, the standard data of 2 I/O modules are transferred to the SafeLOGIC controller and compared with each other there. With the functions provided in SafeDESIGNER, the resulting data can be used for applications up to PL d.

Function DATA_to_SafeDATA is enabled and the register calls take place using SafeDESIGNER. For more detailed information on the calls, see library DATA_to_SafeDATA_SF contained in SafeDESIGNER.

8.6.1 Counter state of the encoder

Name:
Encoder01

This register represents the counter value of the encoder. The register is only active if function DATA_to_SafeDATA is enabled.

Data type	Values
DINT	-2,147,483,648 to 2,147,483,647

8.6.2 NetTime of the counter value

Name:
Encoder01TimeValid

This register represents the NetTime of the most recent valid counter value. The register is only active if function DATA_to_SafeDATA is enabled.

For a description of NetTime Technology, see "NetTime technology" on page 18.

Data type	Values
DINT	-2,147,483,648 to 2,147,483,647

8.6.3 Displaying the SourceRef address

Name:
DTS_SourceRef

This register cyclically displays the SourceRef address set in the configuration. The register is only active if function DATA_to_SafeDATA is enabled.

Data type	Values
INT	-32768 to 32767

8.6.4 Checksum

Name:
DTS_CheckSum

This register contains a checksum formed from the 3 cyclic data points Encoder01, Encoder01TimeValid and DTS_SourceRef. The register is only active if function DATA_to_SafeDATA is enabled.

Data type	Values
INT	-32768 to 32767

8.6.5 SourceRef address

Name:
CfO_DTS_SourceRef

This register contains the acyclically configurable SourceRef address that is sent back by the module as a cyclic data point. The register is only active if function DATA_to_SafeDATA is enabled.

Data type	Values
INT	-32768 to 32767

8.6.6 Constant cycle register

Name:
CfO_DTS_CycleSelect

This register determines the cycle used internally and is not permitted to be changed.

Data type	Value
USINT	2

8.7 NetTime technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (CPU, I/O modules, X2X Link, POWERLINK, etc.).

This allows the time that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a given time.

NetTime TECHNOLOGY

8.7.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with µs timing. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

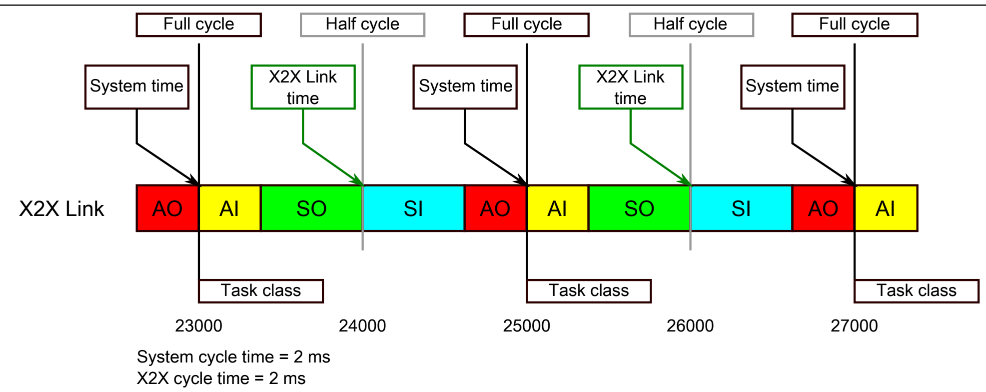
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

8.7.1.1 PLC/Controller data points

The NetTime I/O data points of the PLC or the controller are latched to each system clock and made available.

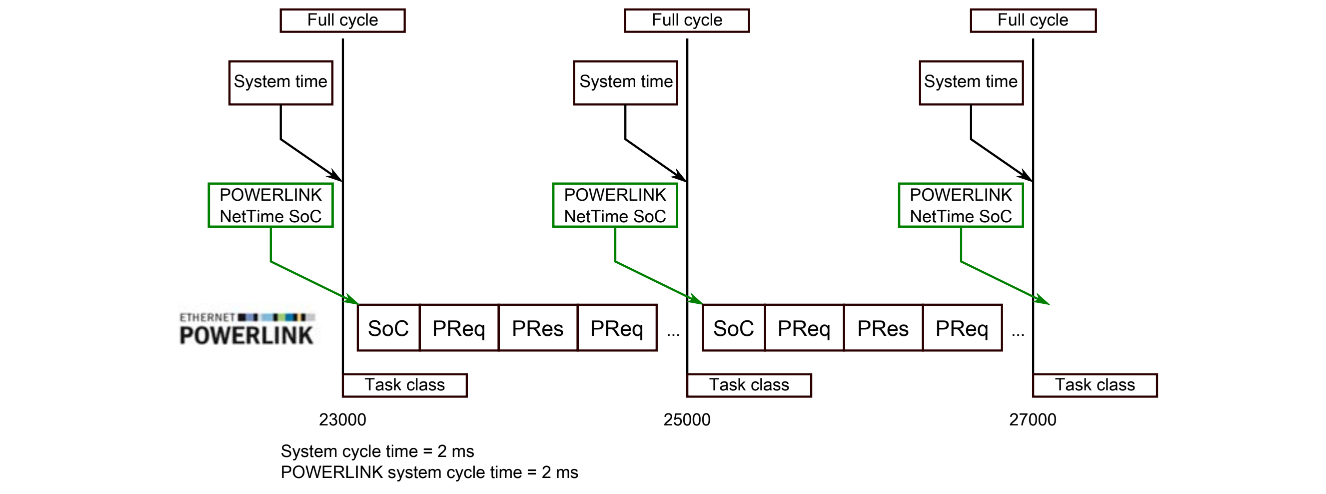
8.7.1.2 X2X Link reference time



The reference time on the X2X Link network is always formed at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference time when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference time returns the value 24000.

8.7.1.3 POWERLINK reference time

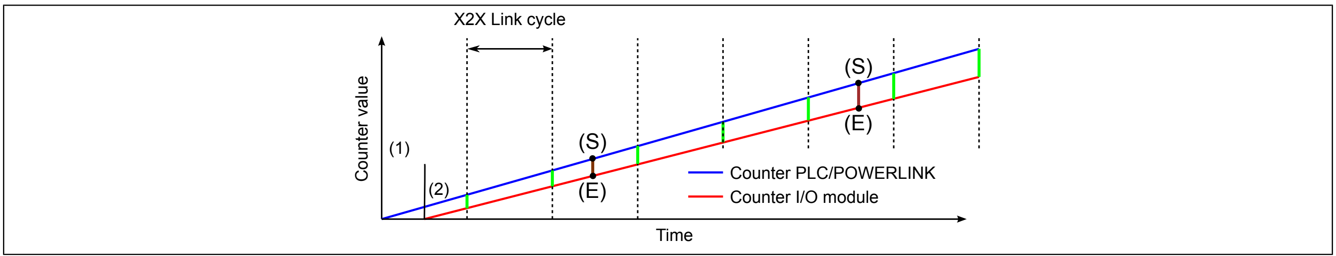


The reference time at POWERLINK is always formed at the SoC (Start of Cycle) of the POWERLINK network. The SoC starts 20 µs after the system tick. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs.

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

8.7.1.4 Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the PLC/POWERLINK (1) and the I/O module (2) start at different times and increase the values at µs intervals.

At the beginning of each X2X Link cycle, the PLC or the POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system time (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

8.7.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the CPU, including this precise time, the CPU can then evaluate the data using its own NetTime (or system time), if necessary.

8.7.2.1 Time-based inputs

NetTime Technology can be used to determine the exact time of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

Information:

The determined time always lies in the past.

8.7.2.2 Time-based outputs

NetTime Technology can be used to specify the exact time of a rising edge at an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

Information:

The specified time must always be in the future and the set X2X Link cycle time must be taken into account for the definition of the time.

8.7.2.3 Time-based measurements

NetTime Technology can be used to determine the exact time of a measurement that has taken place. Both the start and the end time of the measurement can be transmitted.

8.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 μs

8.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
150 μs